Please type a plus sign (+) inside this box [+]

UTILITY PATENT APPLICATION TRANSMITTAL
(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. __042390.P8456__   Total Pages __3__

First Named Inventor or Application Identifier __Randy B. Osborne__

Express Mail Label No. __EL143564497US__

ADDRESS TO:	**Assistant Commissioner for Patents** **Box Patent Application** **Washington, D. C. 20231**

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. __X__   Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. __X__   Specification   (Total Pages __16__)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. __X__   Drawings(s) (35 USC 113)   (Total Sheets __2__)

4. ____   Oath or Declaration   (Total Pages _____)

   a. ___   Newly Executed (Original or Copy)

   b. ___   Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

   i. ___   DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____   Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____   Microfiche Computer Program (Appendix)

7. _____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
    a. _____ Computer Readable Copy
    b. _____ Paper Copy (identical to computer copy)
    c. _____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))

9. _____   a.   37 CFR 3.73(b) Statement (where there is an assignee)

    _____   b.   Power of Attorney

10. _____ English Translation Document (if applicable)

11. _____   a.   Information Disclosure Statement (IDS)/PTO-1449

    _____   b.   Copies of IDS Citations

12. _____ Preliminary Amendment

13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. _____   a.   Small Entity Statement(s)

    _____   b.   Statement filed in prior application, Status still proper and desired

15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. __X__ Other: <u>Unexecuted Declaration and Power of Attorney For Patent Application (4 pgs)</u>

_____

_____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

  ____ Continuation   ____ Divisional   ____ Continuation-in-part (CIP)

    of prior application No: _____

18. **Correspondence Address**

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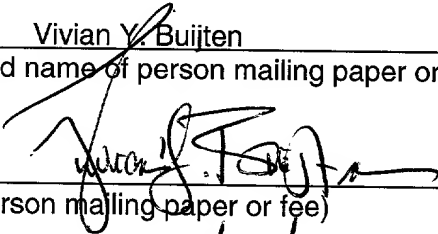
"Express Mail" mailing label number: EL143564497US
Date of Deposit: September 29, 2000

I hereby certify that I am causing the foregoing transmittal, copy thereof,
attached fee transmittal, copy thereof, check in the amount of $744.00,
attached specification and drawings, and an unexecuted Declaration and
Power of Attorney,   to be deposited with the United States Postal Service
"Express Mail Post Office to Addressee" service on the date indicated
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(Typed or printed name of person mailing paper or fee)

_____
(Signature of person mailing paper or fee)

                        9/29/00
_____
(Date signed)

FEE TRANSMITTAL FOR FY 2000

TOTAL AMOUNT OF PAYMENT ($) $ 744.00

Complete if Known:

Application No.	**Not Yet Assigned**
Filing Date	September 29, 2000 (Concurrently Herewith)
First Named Inventor	Osborne, R.
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket No.	042390.P8456

METHOD OF PAYMENT (check one)

1.   [X]   The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number _____ 02-2666 _____

Deposit Account Name _____

[   ]   Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

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2.   __X__   Payment Enclosed:

__X__   Check

_____   Money Order

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FEE CALCULATION

1.   BASIC FILING FEE

Large Entity		Small Entity			
Fee Code	Fee ($)	Fee Code	Fee ($)	**Fee Description**	**Fee Paid**
101	690	201	345	Utility application filing fee	690.00
106	310	206	155	Design application filing fee	_____
107	480	207	240	Plant filing fee	_____
108	690	208	345	Reissue filing fee	_____
114	150	214	75	Provisional application filing fee	_____

SUBTOTAL (1) $ 690.00

2.   EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims 23	− 20** =	3	X 18.00 =	54.00
Independent Claims 3	− 3** =	0	X 78.00 =	00.00
Multiple Dependent			260.00 =	

Or number previously paid, if greater; For Reissues, see below.

Large Entity		Small Entity		
Fee Code	Fee ($)	Fee Code	Fee ($)	**Fee Description**
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 54.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity		Small Entity			
Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,210	241	605	Petition to revive unintentionally abandoned application	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	

Other fee (specify) _____

Other fee (specify) _____

SUBTOTAL (3) $ 00.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Bradley J. Bereznak

Signature _____ Date Sept. 29, 2000

Reg. Number 33,474   Deposit Account User ID _____
(complete if applicable)

UNITED STATES PATENT APPLICATION

for

SYSTEM AND METHOD FOR IMPROVED HALF-DUPLEX BUS PERFORMANCE

Inventors:

Randy B. Osborne

SYSTEM AND METHOD FOR IMPROVED
HALF-DUPLEX BUS PERFORMANCE

RELATED APPLICATION

The present application is related to Serial No. 09/433,653 filed November

5   3, 1999 entitled, "METHOD AND APPARATUS FOR SUPPORTING MULTI-CLOCK

PROPAGATION IN A COMPUTER SYSTEM HAVING POINT-TO-POINT HALF DUPLEX

INTERCONNECT", which application is assigned to the assignee of the present

application.

FIELD OF THE INVENTION

10   The present invention relates generally to the field of computer systems;

more particularly, to methods and apparatus for efficient transfer of data and

information between devices or agents coupled to a bus, data link, or other type

of input/output (I/O) interconnect.

BACKGROUND OF THE INVENTION

15   Manufacturers of semiconductor devices face constant pressure to reduce

the number of interconnects, especially in chipset platforms comprising multiple

semiconductor devices interconnected on a common printed circuit board. Since

the number of pins is a major factor in the costs of inter-chip connections, it is

20   desirable to make such interconnects fast and narrow. This has led to the

development of devices having fewer pins, and pins that can transmit signals

very quickly.

One proposal addressing this problem is to utilize a half-duplex bus with

distributed arbitration for I/O interconnects designed to connect I/O hubs and

25   peripheral component interface (PCI) bridges (e.g., south bridges) to the memory

hub controller (e.g., north bridge). It is well known that in a full-duplex bus, traffic

can flow bi-directionally, simultaneously across separate sets of wires. A half-

duplex bus is one in which there is a single lane of traffic (i.e., one set of wires) that is shared according to some sort of time-multiplexing scheme. A useful analogy is to think of a half-duplex bus as a single-lane bridge spanning across a river or chasm. Flagman positioned at each end signal to the other side to request ownership or use of the bridge in order to allow traffic to traverse in one direction or the other.

A common method to achieve synchronization on a half-duplex bus is via a global clock, also frequently referred to as a common or base clock. Each agent coupled to the bus usually has its own associated request signal line (REQ) used to gain ownership of the bus. Since traffic flow over the bus is always unidirectional, only one side of the bus has ownership of the bus at any given time. Each agent executes the same arbitration algorithm; asserting its request signal to convey its request to a remote agent; sampling the request signal driven by the remote agent; and then choosing which agent to grant ownership to based on the local and remote requests. Thus, in a half-duplex bus link, both ends contend for the shared bus resource.

In a typical I/O environment in which a half duplex a bus is deployed, one end of the link usually connects to a memory controller. The vast majority of traffic comprises memory reads and writes generated by devices connected to the I/O bridge and targeting the memory coupled to the memory controller. In such a system, three types of requests normally contend for ownership of the link: (1) write transfers (address plus data) upstream to the memory controller; (2) read requests (address plus size); and (3) read returns (address plus data) downstream to the requesting agent.

Data writes and read returns are very similar in that the both have a long latency and both are unidirectional "fire and forget" transfers. But a memory read operation is quite different. A successful memory read operation requires a

complete round-trip over the bridge; that is, a read request must first travel upstream to the memory controller, where the request is serviced, followed by a return of the read data downstream back to the requesting agent.

The rate of read returns is often limited by the rate at which read requests

5   travel upstream. Under heavy loading conditions, particularly involving many downstream read returns, there can be a long delay before traffic flow across the link is turned around to permit an upstream read request. If the latency period is too long, the memory controller will run out of pending requests, and thus experience a momentary break in the pipelining of read returns. Failure to allow a

10   read request upstream in a timely manner can therefore result in a "bubble" in the read return traffic, with a corresponding reduction in read bandwidth.

Accordingly, what is needed is a method or protocol that permits more efficient utilization of the half-duplex bus resource.

15

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed

which follows and from the accompanying drawings, which however, should not

be taken to limit the invention to the specific embodiments shown, but are for

5   explanation and understanding only.

Figure 1 is a diagram of an interconnect system in which agents

communicate information over a shared bus in accordance with one embodiment

of the present invention.

10   **Figure 2** is a timing diagram showing signal transmission across a half-

duplex bus in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

An system and method for improved half-duplex bus performance under heavy loading is described. In the following description, numerous details are set forth, such as specific system configurations, algorithms, signal lines, etc., in

5   order to provide a thorough understanding of the invention. It will be clear, however, to one skilled in the art, that these specific details may not be needed to practice the present invention.

With reference to Figure 1, there is shown an interconnect system comprising a pair of bus agents 11 and 19 (agents "A" & "B", respectively)

10   coupled to a common bus 14. (Numeral 14 is used to denote the actual signal lines or wires used to transfer data between two agents. However, it should be understood that the term "bus" is sometimes used by practitioners to collectively denote lines 14-17; that is, all of the lines connecting the respective agents. In the context of the present discussion, each of these lines is referred to

15   separately.) Each agent coupled to the bus executes exactly the same distributed arbitration algorithm. For example, in one embodiment, bus 14 may comprise a half-duplex bus with distributed arbitration. Each agent includes an arbiter that operates in accordance with a predetermined arbitration algorithm. In Figure 1, agent 11 includes an associated arbiter 12, and agent 19 includes an associated

20   arbiter 18. In a typical system configuration, agent 11 may comprise a memory controller coupled to a main or cache memory, and agent 19 may comprise an I/O bridge device.

Both agents are also coupled via associated request signal lines 15 and 16. Both agents monitor these request signal lines to determine if a request

25   signal from a remote agent has arrived. The request signals are used by the agents to gain ownership of the bus for transmission of data and information. In Figure 1 an upstream request (REQ_{up}) is made by agent 19 to gain ownership of

bus 14 for a transfer of information in a direction from agent 19 to agent 11. Likewise, a downstream request (REQ$_{dn}$) is made by agent 11 to gain ownership of bus 14 for a transfer of information in a direction from agent 11 to agent 19. By way of example, agent 19 (e.g., an I/O bridge) asserts line 16 prior to sending

5   a read request across half-duplex bus 14 to agent 11 (e.g., a memory controller). In the same manner, agent 11 would assert line 15 prior to sending data of a read return back to requesting agent 19.

Operations on bus 14 are synchronized by a common or global clock signal, i.e., GCLK, (not shown).

10   In accordance with one embodiment of the present invention, a preempt signal line 17 is connected between the arbitration units 12 and 18 of the two agents. (It is appreciated that the "#" symbol denotes that the preempt signal is asserted when the voltage potential or logic level of the line is low.) Preempt signal 17 is utilized in the present invention as a way for the downstream end to

15   convey the presence of a pending read request to the upstream end. As will be described in more detail shortly, preempt signal 17 provides a way for the distributed arbiters of the upstream and downstream ends to synchronize and dynamically preempt a read return.

Under heavy loading conditions the arbiters operate according to a

20   protocol that improves efficiency by minimizing bus turnarounds, while at the same time ensuring that enough read requests get transferred upstream in a timely manner to avoid read starvation and the resultant loss in read bandwidth. The preempt signal 17 implements the idea of a "time-slice", wherein bus traffic from the upstream to the downstream end of the bus bridge is occasionally

25   interrupted to allow read requests to cross the bridge, thereby ensuring that the bus does not go idle due to read starvation.

The present invention is not limited to a time-slice of a particular duration. In other words, the time-slice can vary depending on system considerations. For example, the preempt signal may be used to implement a time-slice which immediately and interrupts traffic flow over the bus bridge to allow a read request

5   across the bus in the opposite direction as soon as it appears at one end of the bus. This example represents an extreme case, since granting read requests in this manner would produce a large number of bus turnarounds, i.e., reversing the direction of bus traffic, which would result in an inefficient utilization of the bus resource. At the other extreme, is the case where the time slice is intentionally

10   made very long. But the problem with making the time slice too long is that it leads to the starvation problem previously discussed. That is, if the time slice is very large, there is a risk that the bridge will become idle due to not enough pending read requests being serviced by the memory controller for downstream return across the bus bridge. Therefore, the present invention achieves

15   optimized utilization of the bus by a preemption algorithm that balances the foregoing concerns for a particular system application.

Note that if only memory writes were transmitted from both directions it would make sense to make the time-slice the very long since writes are not sensitive to latency and they are not round-trip transactions.

20   The preempt signal provides the arbiter associated with the agent at one end of the bus with additional information regarding the request type pending at the opposite end. In the example of Figure 1, preempt signal 17 is asserted by agent 19 when it has a read request waiting to be sent over the bus bridge. Arbiter 12 associated with agent 11 can respond to preempt signal 17 in a

25   number of different ways, depending on the particular preemption algorithm being implemented. For instance, arbiter 12 may determine that the number of requests pending is below a certain number, warranting that it relinquish its

current ownership of the bus to the remote agent. The key concept is that the preemption signal provides information to a remote agent regarding a pending read request at the opposite end of the unidirectional bus. Depending on the number of requests the remote agent is currently servicing or that it has queued

5   for delivery downstream across the bus, that agent can decide to interrupt the stream of downstream traffic going over the bus.

A wired-OR signal connection, or its equivalent, is one possible way of identifying a pending request at the downstream end as a read request for which preemption is to occur. To determine if the starvation may occur, the upstream

10 end examines the queue of read requests sent from the downstream end that is awaiting service by the memory controller. If the queue is below the predetermined threshold, e.g., empty, then read starvation may occur. In response, the upstream arbiter can elect a suitable point at which to preempt the read return, e.g., at a cacheline boundary. To synchronize the downstream

15 arbiter to the same preemption point, the upstream arbiter removes (i.e., de-asserts) its request signal. Upon observing the upstream end's request signal being de-asserted, the downstream arbiter considers the read return terminated and agrees to turnaround the direction of traffic flow on the bus.

It should be understood that the preemption mechanism may comprise

20 more than a single wire or signal. The specific way that the preemption mechanism is implemented is not essential to the present invention. Rather, the important concept involves the use of the preemption mechanism to signal the type of request that is pending at the opposite end of the link for the purpose of solving the problem of read starvation.

25 To recapitulate, the preempt signal is asserted when there are a certain number of read requests queued up at one end of the bus bridge (assuming that the agent at that end does not presently have ownership of the bus). The

preempt signal is asserted to notify the remote agent at the other end of the bus (via the preemption algorithm) that there are a number of read requests pending to be sent across the bus in the opposite direction. The upstream agent receiving the preempt signal examines the traffic loading at its end in determine whether it

5   is appropriate to relinquish ownership of the bus to allow a number of read requests across the bus in the opposite direction to avoid read starvation. After a number of read requests have been sent across the bus in the upstream direction, the upstream agent may then request ownership of the bus to once again send read return data downstream to the remote agent.

10   Note that the control algorithm may vary; for example, the downstream agent can make its own decision about what type of traffic to send over the bus after it asserts the preemption signal. Likewise, the upstream agent may decide to only allow a certain number of read requests to cross the bridge following the preemption request. For example, the downstream end may try to make the time-

15   slice long by sending over all of its pending read requests along with several writes in order to amortize the turnaround penalty. It is appreciated that this is simply an implementation detail that may be parameterized utilizing an ordinary time-slice counter. For instance a certain number of clocks may be loaded into the counter to set the duration of time-slice.

20   Figure 2 is an exemplary timing diagram that illustrates how the downstream agent may preempt the upstream agent's return of read data. In the example of Figure 2, the preempt signal is a unidirectional signal having a direction opposite to the direction data is currently flowing across the bus. For example, if traffic is flowing from agent "A" to agent "B", the preempt signal is

25   only allowed in the opposite direction; namely, from agent "B" to agent "A". In this example, there is a one clock delay before the preempt signal can be asserted following a turnaround of data flow across the bus.

Viewing Figure 2 in conjunction with Figure 1, it can be seen that the internal logic of arbiter 18 first recognizes that it has a read request to be sent upstream between clock edges CLK_0 and CLK_1. At clock edge CLK_0 agent 11 has ownership of bus 14 and is sending read return data downstream to agent 19

5   via bus wires PD. This is evident by the high level of REQ_{dn} and the presence of read return data on wires PD in Figure 2. In the following clock period, between clock edges CLK_1 and CLK_2, the REQ_{up} signal is asserted by raising signal line 16 to a logical high level. In the same clock period PREEMPT# is asserted low by agent 19 to notify agent 11 that it has a pending read request. In this case, the

10   high-to-low transition of PREEMPT# is triggered by sampling both REQ_{dn} and $REQ_{up(internal)}$ high at the rising edge of CLK_1.

Agent 11 samples REQ_{up} and PREEMPT# at the rising edge of CLK_2. In response, arbiter 12 de-asserts REQ_{dn} and terminates read return traffic flow to initiate a turnaround in the direction of traffic flow on bus 14. The turnaround

15   occurs between clock edges CLK_3 and CLK_4. As explained earlier, the particular preemption algorithm being implemented by arbiter 12 determines the exact time when the upstream end relinquishes ownership of the bus.

At clock edge CLK_4 the downstream end (agent 19) gains ownership of the bus and begins transmitting its read request to the upstream end over the PD

20   signal lines. Arbiter 18 grants ownership of the bus back to the upstream end between clock edges CLK_6 and CLK_7 by de-asserting REQ_{up}, whereupon the upstream end (agent 11) once again begins sending read return data across bus 14 commencing at CLK_6. (Note that the downstream agent sampled REQ_{dn} high at the rising edge of CLK_4.)

25   In the case where the transmitting agent sends header information within a given base clock signal, parity information encoded using a header parity function is sent on the parity signal lines. (Practitioners familiar in the art will

appreciate that within each common or base clock, which is used solely for synchronization, there is usually a data clock which run significantly faster, e.g., 4x, 8x, etc.).

It should be appreciated that the preempt signal could be implemented and any one of a number of different ways. In one embodiment, the preempt signal could be implemented as a single wire that is always owned by the downstream agent. In another embodiment, the signal may be implemented to allow for two-way preemption; e.g., where agent "A" may preempt agent "B" and vice-versa. The illustrations of Figures 1 and 2 should therefore not be considered to limit the scope of the present invention.

I claim:

1   1.   A method of operation for a half-duplex bus comprising:

2   asserting a preempt signal by a first agent to indicate that the first agent

3 has a read request pending for transmission over the half-duplex bus;

4   sampling the preempt signal by a second agent; and

5   relinquishing ownership of the half-duplex bus by the second agent

6 responsive to the preempt signal.

1   2.   The method of claim 1 further comprising:

2   sending the read request over the half-duplex bus from the first agent to

3 the second agent.

1   3.   The method of claim 1 further comprising:

2   returning ownership of the half-duplex bus back to the second agent;

3   sending read data over a the half-duplex bus from the second agent to the

4 first agent.

1   4.   The method of claim 3 wherein the read data is associated with the read

2 request.

1   5.   The method of claim 1 wherein the second agent comprises a memory

2 controller.

1   6.   The method of claim 1 wherein the first agent comprises an input/output

2 device.

1   7.   A method of operation for a half-duplex bus comprising:

2   sending a read return over the half-duplex bus from a first agent to a

3   second agent;

4   signaling the first agent by the second agent that the second agent has a

5   read request pending;

6   electing by the first agent a suitable point at which to preempt the read

7   return;

8   granting ownership of the half-duplex bus to the second agent;

9   sending the read request from the second agent to the first agent over the

10   half-duplex bus; and

11   returning ownership of the half-duplex bus to the first agent.

1   8.   The method of claim 7 wherein the signaling step comprises:

2   asserting a request signal and a preempt signal by the second agent;

3   sampling the request signal and the preempt signal by the first agent.

1   9.   The method of claim 7 further comprising:

2   determining by the first agent that a threshold indicative of imminent read

3   starvation has been exceeded.

1   10.   The method of claim 7 wherein the suitable point comprises a cacheline

2   boundary.

1   11.   The method of claim 7 wherein the granting ownership and returning

2   ownership steps comprise a one clock period turnaround.

1   12.   The method of claim 7 wherein the first agent comprises a memory

2   controller.

1   13.   The method of claim 12 wherein the second agent comprises an

2   input/output bridge device.

1   14.   The method of claim 7 wherein the second agent includes an arbiter that

2   executes an arbitration protocol.

1   15.   The method of claim 14 wherein the arbiter of the first agent also

2   executes a preemption algorithm to elect the suitable point.

1   16.   A computer system comprising:

2   a half-duplex bus;

3   first and second agents coupled to the half-duplex bus, each having an

4   arbiter that follows an algorithm to determine ownership of the half-duplex bus;

5   first and second request lines coupled between the first and second

6   agents, the first request line being asserted by the first agent to request

7   ownership of the half-duplex bus from the second agent, and the second request

8   line being asserted by the second agent to request ownership of the half-duplex

9   bus from the first agent in accordance with the algorithm; and

10   a preempt signal that is asserted by the second agent to indicate to the

11   first agent that the second agent has a certain type of request pending.

1   17.   The computer system of claim 16 wherein the certain type of request is a

2   read request.

1   18. The computer system of claim 17 wherein the second agent asserts the

2   preempt signal during a current read return from the first agent to the second

3   agent.

1   19. The computer system of claim 18 wherein the arbiter of the first agent

2   responds to the preempt signal in accordance with a preemption algorithm that

3   determines a suitable point to relinquish ownership of the half-duplex bus to the

4   second agent.

1   20. The computer system of claim 19 wherein the suitable point comprises a

2   cacheline boundary.

1   21. The computer system of claim 16 wherein the first agent comprises a

2   memory controller.

1   22. The computer system of claim 21 wherein the second agent comprises

2   an input/output device.

1   23. The computer system of claim 19 wherein execution of the preemption

2   algorithm by the arbiter of the first agent causes the first agent to determine

3   whether a queue of read requests awaiting service by the first agent is below a
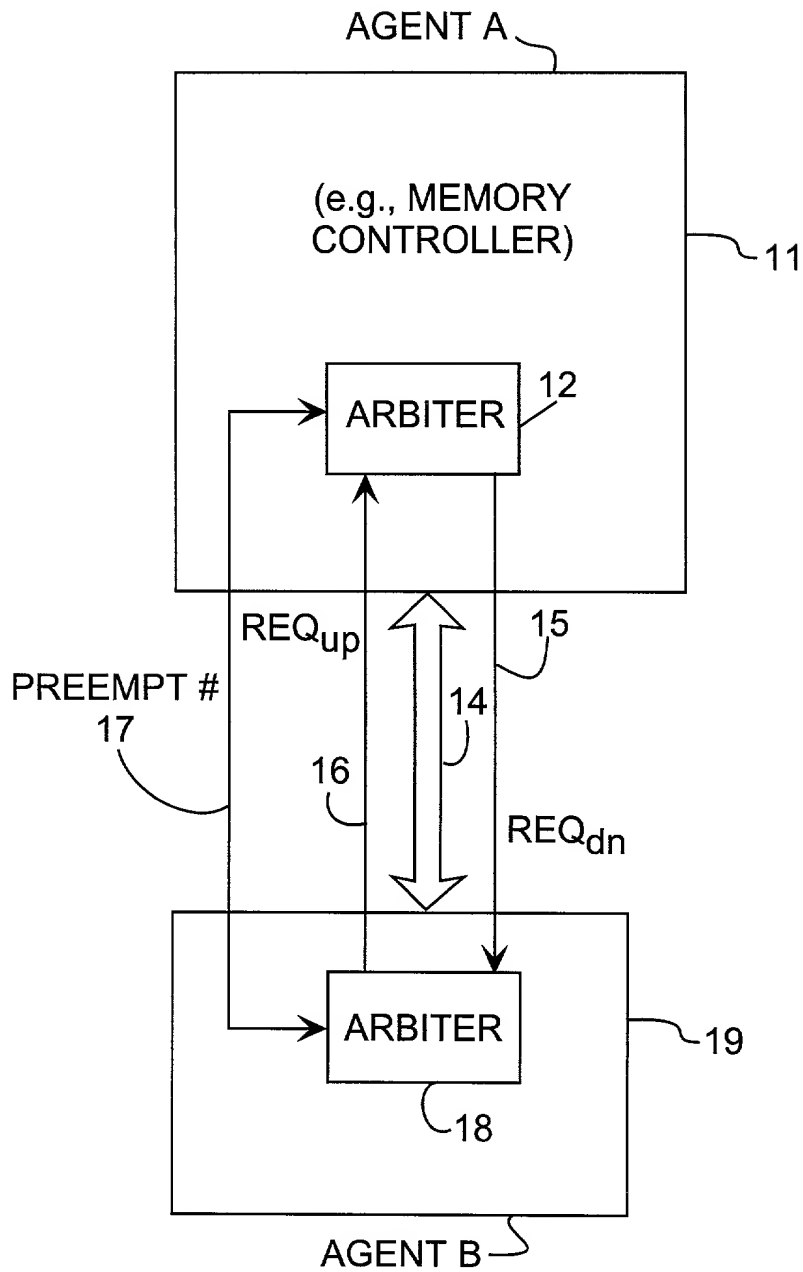
4   predetermined threshold.

<u>ABSTRACT OF THE DISCLOSURE</u>

A method for dynamic preemption of read returns over a half-duplex bus during heavy loading conditions involves asserting a preempt signal by a first agent to indicate that the first agent has a read request pending for transmission

5 over the half-duplex bus. A second agent then samples the preempt signal sent by the first agent. The second agent relinquishes ownership of the half-duplex bus responsive to the preempt signal to allow the read request to be sent across the half-duplex bus.

AGENT A

(e.g., MEMORY
CONTROLLER)   11

ARBITER   12

REQ$_{up}$ 15

PREEMPT #   14
17
                        16   REQ$_{dn}$

ARBITER   19

18

AGENT B

FIG. 1

FIG. 2

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**SYSTEM AND METHOD FOR IMPROVED
HALF-DUPLEX BUS PERFORMANCE**

the specification of which

__XX__	is attached hereto.
_____	was filed on _____ as
	United States Application Number _____
	or PCT International Application Number_____
	and was amended on _____.
	(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date

Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned

Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to __Bradley J. Bereznak__, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct
telephone calls to __Bradley J. Bereznak__, (408) 720-8300.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor __Randy B., Osborne__

Inventor's Signature _____ Date _____

Residence ____Beaverton, Oregon____ Citizenship ____Canada____
(City, State)   (Country)

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1)   Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2)   The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b)   Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1)   It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2)   It refutes, or is inconsistent with, a position the applicant takes in:

(i)   Opposing an argument of unpatentability relied on by the Office, or

(ii)   Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c)   Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1)   Each inventor named in the application;

(2)   Each attorney or agent who prepares or prosecutes the application; and

(3)   Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d)   Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.